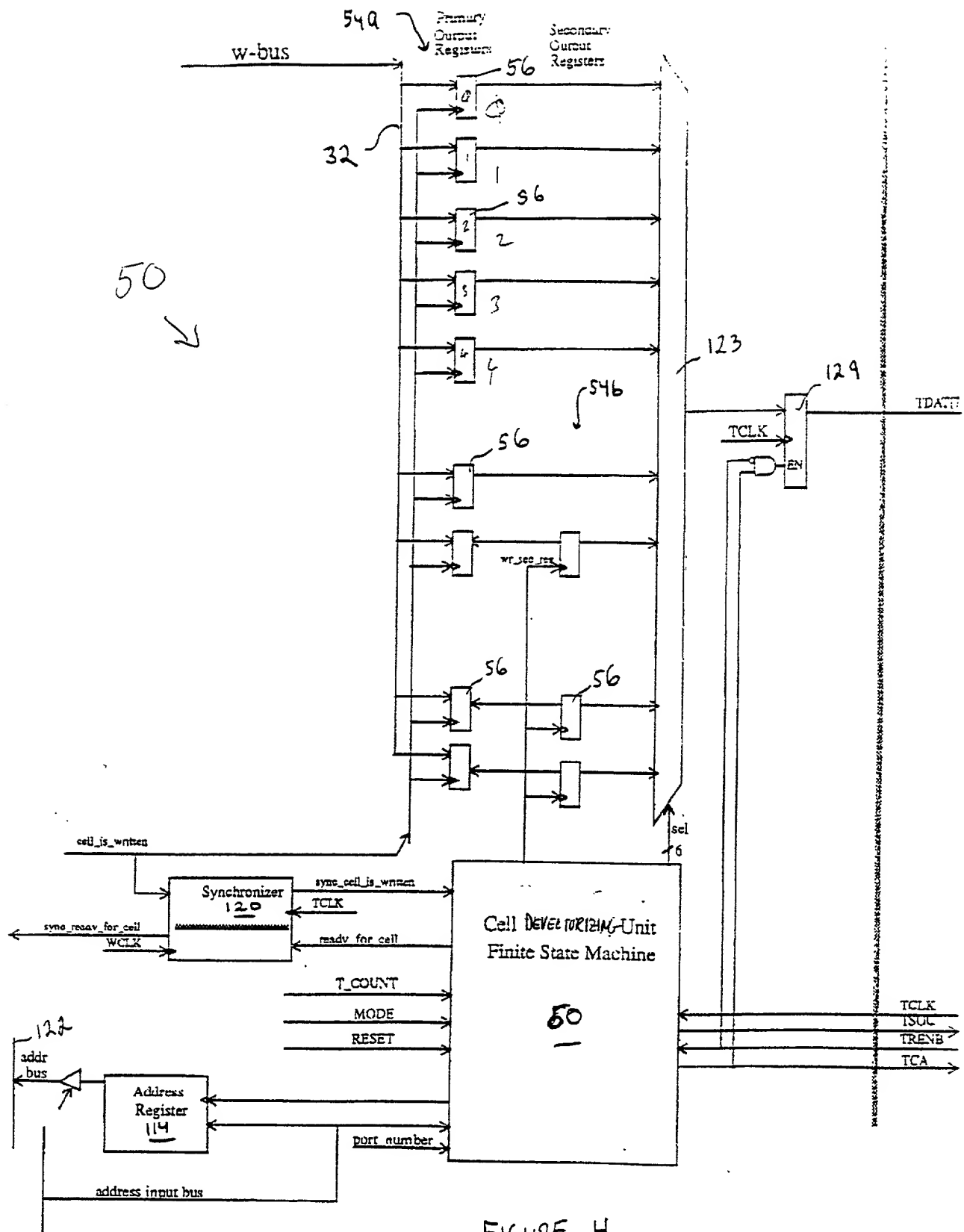


Figure 2

Figure 2 is a block diagram of the Cell Vectorizing Unit Finite State Machine (58). The diagram shows the internal structure of the unit, including Secondary Input Registers (54b) and Primary Input Registers (54a). It details the flow of data from RDAT[7:0] through a multiplexer (56a) and a series of registers (56b, 56c, 56d, 56e, 56f, 56g, 56h, 56i, 56j, 56k, 56l, 56m, 56n, 56o, 56p, 56q, 56r, 56s, 56t, 56u, 56v, 56w, 56x, 56y, 56z) to the w-bus (32) and byte enable signals. The unit also includes a Synchronizer (120) and an Address Register (114). Handwritten annotations include '46' and '56'.

Figure 3.

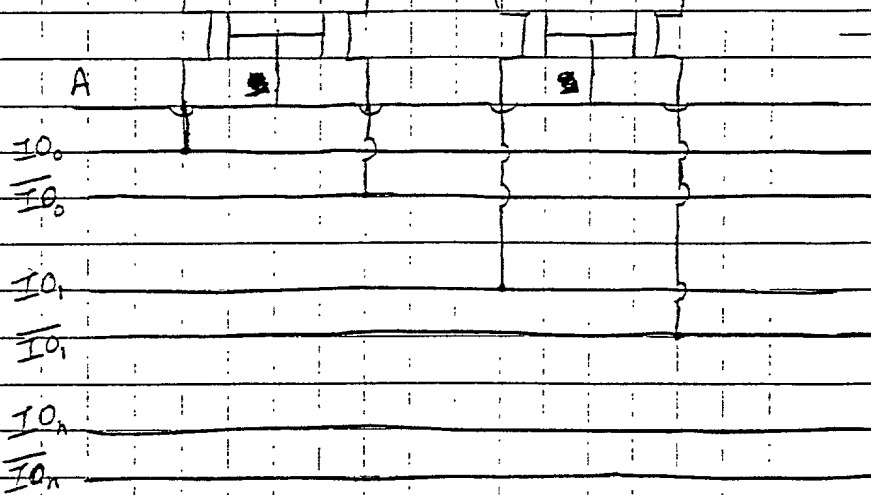
109270" 9603T560



5	a
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09916096.072601

5b
figure
BL0 BL1 BL1 BL1



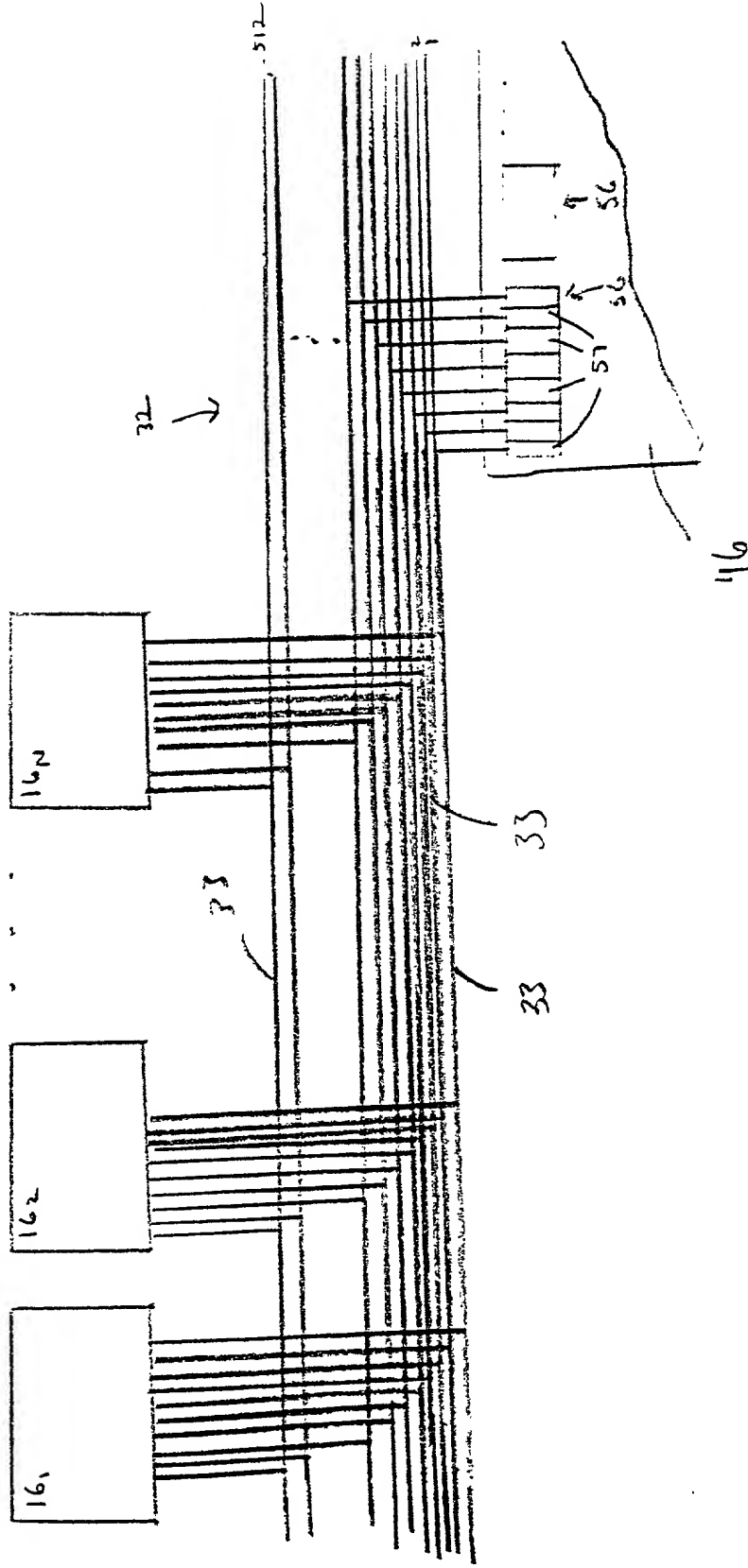


FIGURE 6

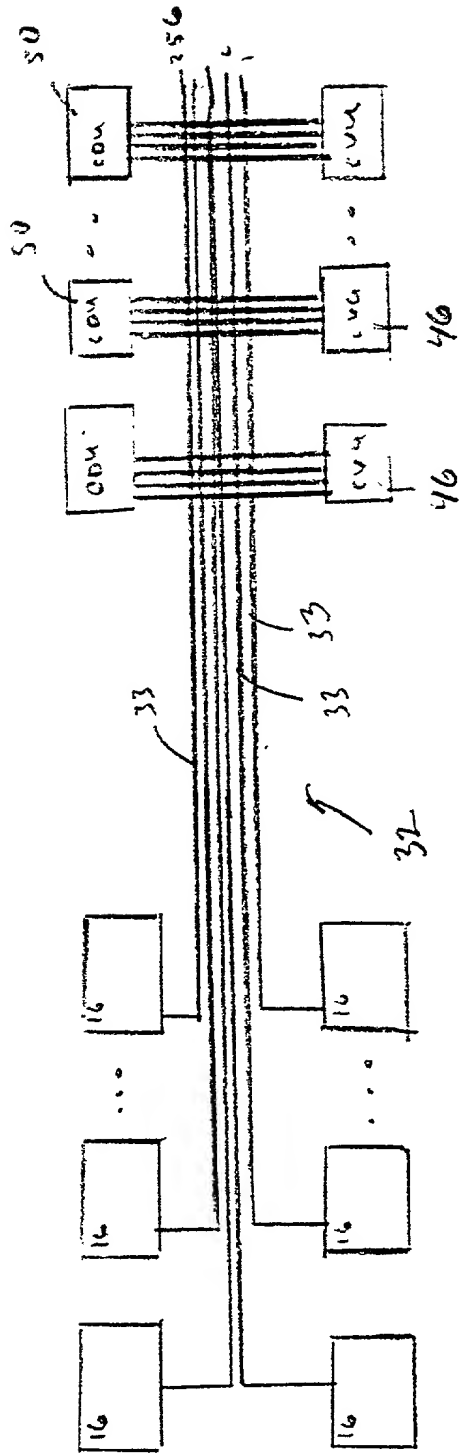


FIGURE 7